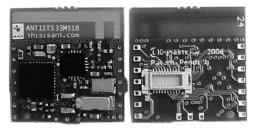


AT3 RF Transceiver Module

FEATURES

- 2.4GHz worldwide ISM band
- 20mm x 20mm drop-in module
- SensRcore[™] development platform
- Ultra low power operation
- Simple sync/async serial interface
- Integrated F antenna
- Broadcast, acknowledged, or burst data transmissions
- ANT channel combined message rate up to 180Hz (8byte data payload)
- Minimum message rate per ANT channel 0.5Hz
- Burst transfer rate up to 20Kbps (true data throughput)
- 1 Mbps RF data rate
- Up to 1/4/8 ANT channels
- 125 selectable RF channels
- Up to 3 public, managed and/or private networks
- 2.0V to 3.6V supply voltage range
- -40°C to +85°C operating temperature
- FCC test ready
- RoHS compliant

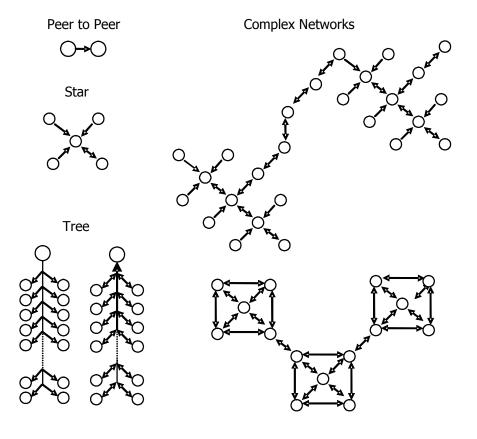




FAMILY MEMBERS

- ANT11TS33M4IB / ANT11TS33M5IB 8 ANT channels, SensRcore™
- ANT11TS53M4IB 4 ANT channels, SensRcore™
- ANT11TS63M4IB 1 ANT channel, SensRcore™

ANT11TR13M4IB 8 ANT channels



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Notices and Restricted Use Information

Restricted use of ANT RF Transceiver Modules.

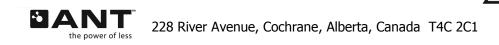
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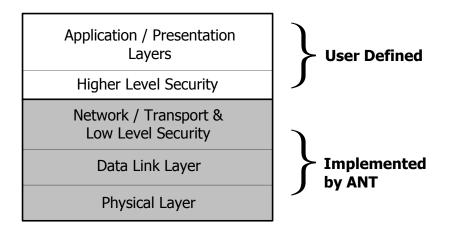
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ANT[™] Overview

ANT[™] is a practical wireless sensor network protocol running on 2.4 GHz ISM band. Designed for ultra low power, ease of use, efficiency and scalability, ANT easily handles peer-to-peer, star, tree and practical mesh topologies. ANT provides reliable data communications, flexible and adaptive network operation and cross-talk immunity. ANT's protocol stack is extremely compact, requiring minimal microcontroller resources and considerably reducing system costs.

ANT provides carefree handling of the Physical, Network, and Transport OSI layers. In addition, it incorporates key low-level security features that form the foundation for user-defined, sophisticated, network-security implementations. ANT ensures adequate user control while considerably lightening computational burden in providing a simple yet effective wireless networking solution.



ANT supports public, managed and private network architectures with 2³² uniquely addressable devices possible, ensuring that each device can be uniquely identified from each other in the same network.

ANT is proven with an installed base of over two million nodes in ultra low power sensor network applications in sport, fitness, home and industrial automation. The ANT solutions are available in chips, chipsets and modules to suit a wide variety of application needs.

A complete description of the ANT message protocol is found in the ANT Message Protocol and Usage document. The serial interface details are provided in the Interfacing with ANT General Purpose Chipsets and Modules document.



1

AT3 Modules

The AT3 drop-in modules are intentionally engineered for ease of use, scalability and lowest power consumption. AT3 modules are based on the chipset combining MSP430f22x2/4, the ultra low power microcontroller (MCU) from Texas Instrument, and nRF24L01, the ultra low power radio chip from Nordic Semiconductor. Integrated with an F antenna, AT3 modules reduce the need for RF design expertise. SensRcore[™], an easy-to-use design platform to build wireless sensors, is equipped in most of AT3 modules.

AT3 family of modules provides a comprehensive solution to the requirements of building a wireless sensor network consisting of nodes from simple sensors to complex hubs or control nodes. A common pinout and 20 x 20mm footprint enables easy network development, upgrade, migration and maintenance.

| Module | Description |
|---------------|---|
| ANT11TS33M4IB | 8 ANT channels, SensRcore with 8 data channels, surface mountable, industrial temperature range |
| ANT11TS33M5IB | 8 ANT channels, SensRcore with 8 data channels, Molex connector, industrial temperature range |
| ANT11TR13M4IB | 8 ANT channels, surface mountable, industrial temperature range |
| ANT11TS53M4IB | 4 ANT channels, SensRcore with 6 data channels, surface mountable, industrial temperature range |
| ANT11TS63M4IB | 1 ANT channel, SensRcore with 4 data channels, surface mountable, industrial temperature range |

Four standard AT3 modules are delivered on one common hardware platform:

The AT3 module has been pre-tested by a FCC registered lab to comply with the requirements for FCC CFR47 and other applicable standards for Intentional Radiators.

1.1 SensRcore[™] Platform

SensRcore is a wireless sensor development platform that is equipped with most AT3 modules. When using sensRcore to develop a wireless sensor, both analog and digital sensors can be directly connected to the ANT MCU. The normally required firmware development is replaced by writing a simple SensRcore script. An application host MCU could be eliminated from the system design. The result is a reduced component cost, size, power and the shortened development cycle of the target sensor device.

When AT3 modules are operated in sensRcore mode, the channel configuration parameters are stored in non-volatile memory and are enabled upon power-up. When I/O pins are configured as digital inputs or outputs, the electrical requirements are the same as all other signaling pins. When I/O pins are configured as analog inputs, different signal ranges can be selected with different reference voltages. The reference voltages available are V_{CC} , 2.5V, and 1.5V. Signals that exceed the specified reference level will be read by the A/D as a maximum value. Signal levels should not exceed V_{CC} . Each AIOx pin can be used as an analog input or a digital I/O pin; each IOx pin can be used only as a digital I/O pin. I/O pins that are not being used in a specific SensRcore mode configuration should be left configured as digital inputs, which is the default setting.

ANT sensRcore scripts consist of ANT messages and commands. Please refer to "ANT Message Protocol and Usage" and "SensRcore Messaging and Usage". The script can be generated by using the software tool *SensRware*. There are 200 bytes available in the non volatile memory for SensRcore script.



1.2 Pin Assignment

The ANT11Txx3MxIB module contains a dual-chip ANT implementation. The ANT MCU contains the ANT protocol stack along with the ANT serial interface. The radio chip is Nordic Semiconductor's nRF24L01. The module may be connected to the user's host controller using the 17 pin-out assignment (surface mount) style or the 20-pin Molex header connection style provided below:

| Surface Mount Pin | Molex Header Pin | Pin Name | Async Mode | Sync Mode | SensRcore Mode | Description |
|-------------------------|------------------------|-------------------------|----------------------------|----------------------------|--|---|
| 1 | 6 | TIE_GND1 | GND | GND | GND | Not used, must be tied to ground |
| 2 | 10 | RESET | RESET | RESET | RESET | Active low reset pin |
| 3 | 1 | V _{CC} | V _{CC} | V _{CC} | V _{cc} | Power supply source |
| 4 | 19 | TIE_GND2 | GND | GND | GND | Power supply ground |
| 5 | 8 | 105 | Tie to GND | Tie to GND | 105 | SensRcore mode -> digital input/output |
| 6 | 17 | SUSPEND / SRDY /AIO0 | SUSPEND | SRDY | AIOO | ASync -> Suspend control Sync -> Serial port ready SensRcore -> Analog/Digital input / output |
| 7 | 15 | SLEEP/ MRDY /AIO1 | SLEEP | MRDY | AIO1 | Async -> Sleep mode enable Sync -> Message ready indication SensRcore -> Analog/Digital input / output |
| 8 | 13 | IO7 | Tie to GND | Tie to GND | I07 | SensRcore -> Digital input / output |
| 9 | 11 | PORTSEL | PORTSEL (Tie to GND) | PORTSEL (Tie to V_{CC}) | Tie to V _{CC} for custom Tie to GND for demo | Asynchronous or synchronous port select SensRcore -> Demo script or user scripts |
| 10 | 7 | BR2/SCLK/ DevSel2 | BR2 | SCLK | DevSel2 | Async -> Baud rate selection Sync -> Clock output signal SensRcore -> Configuration selection |
| 11 | 4 | TXD0/SOUT/ IO6 | TXD0 | SOUT | IO6 | Async -> Transmit data signal Sync -> Data output SensRcore -> Digital input / output |
| 12 | 3 | RXD0/SIN/AIO2 | RXD0 | SIN | AIO2 | Async -> Receive data signal Sync -> Data input SensRcore -> Analog/Digital input / output |
| 13 | 5 | BR1/SFLOW/ DevSel1 | BR1 | SFLOW | DevSel1 | Async -> Baud rate selection Sync -> Bit or byte flow control select SensRcore -> Configuration selection |
| 14 | 9 | BR3/DevSel3 | BR3 | Tie to GND | DevSel3 | Async -> Baud rate selection Sync -> Tie low SensRcore -> Configuration selection |
| 15 | 14 | AIO3 | Tie to GND | Tie to GND | AIO3 | SensRcore -> Analog/Digital input / output |
| 16 | 12 | AIO4 | Tie to GND | Tie to GND | AIO4 | SensRcore -> Analog/Digital input / output |
| 17 | 2 | RTS/SEN/IOSEL | RTS | SEN | IOSEL (Tie to GND) | Async -> Request to send Sync -> Serial enable signal SensRcore -> IOSEL tie low |
| | 16, 18, 20 | NC | NC | NC | NC | No connection |

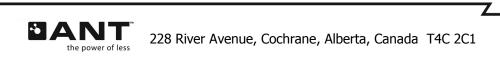
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1.3 Asynchronous Baud Rate

The baud rate of the asynchronous communication is controlled by the speed select signals BR1, BR2 and BR3. The table below shows the relationship between the states of the speed select signals and the corresponding baud rates.

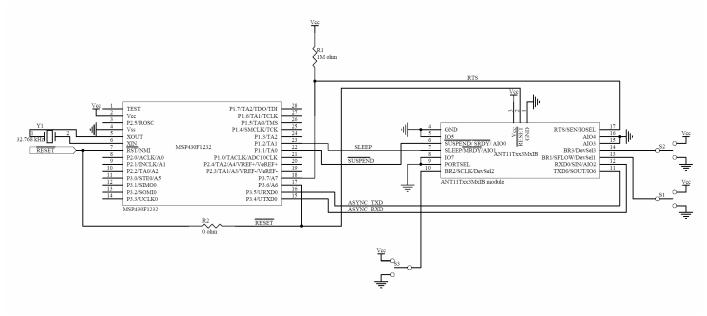
| BR3 | BR2 | BR1 | Baud Rate |
|-----|-----|-----|-----------|
| 0 | 0 | 0 | 4800 |
| 0 | 1 | 0 | 19200 |
| 0 | 0 | 1 | 38400 |
| 0 | 1 | 1 | 50000 |
| 1 | 0 | 0 | 1200 |
| 1 | 1 | 0 | 2400 |
| 1 | 0 | 1 | 9600 |
| 1 | 1 | 1 | 57600 |



2 Sample Designs

Samples 3.1, 3.2, and 3.3 show the proper electrical connectivity of an ANT11TxxxMxIB module to an application's host microcontroller. The three reference designs use the 17 pin-out assignment connection style.

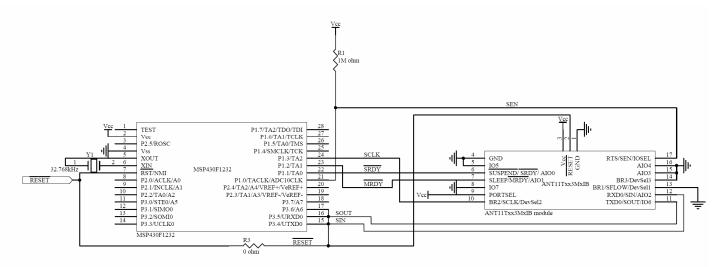
2.1 Async Mode



Notes:

- Module RXD and TXD connected directly to hardware USART of microcontroller.
- The illustrated switches on the baud rate selection pins (BR1, BR2, and BR3) are for ease of use only. The Baud rate selection pins may be connected directly to the logic level of interest.
- R2 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

2.2 Byte Sync Mode

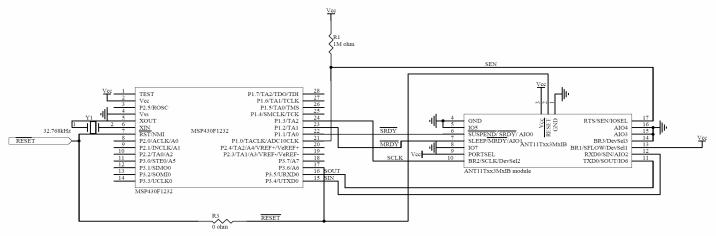




Notes:

- Module SOUT and SIN connected directly to hardware USART of microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

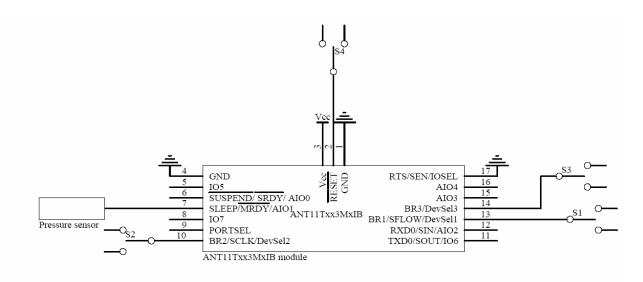
2.3 Bit Sync Mode

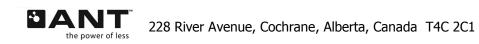


Notes:

- All interface signals are connected directly to I/O pins on the microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

2.4 SensRcore[™] Mode (pressure sensor configuration)





3 Electrical Specifications

| Absolute Maximum Ratings | |
|---|-------------------------|
| Voltage applied at V_{CC} to V_{SS} | -0.3V to +3.6V |
| Input voltage at any pin | -0.3V to V_{CC} +0.3V |
| Diode current at any pin | ±2mA |
| Operating temperature | -40°C to +85°C |
| Storage temperature | -40°C to +85°C |

Note: Stress exceeding one or more of the absolute maximum ratings may cause permanent damage to the chipsets.

| Symbol | Parameter (condition) | Notes | Min | Тур | Max | Units |
|------------------------------|--|-------|---------------------------|------|-----------------|----------|
| | Operating conditions | | | | | |
| V _{CC} | Supply voltage | | 2.0 | 3.0 | 3.6 | V |
| TEMP | Operating temperature | | -40 | 25 | +85 | ٥C |
| | Digital input pin | | | | | |
| V _{IH} | HIGH level input voltage | | 1.9 | | V _{CC} | V |
| V _{IL} | LOW level input voltage | | V _{SS} | | | V |
| | Digital output pin | | | | | |
| V _{OH} | HIGH level output voltage (I_{OH} =-0.5mA) | | V _{CC} - 0.25 | | V_{CC} | V |
| V _{OL} | LOW level output voltage ($I_{OL}=0.5mA$) | | V _{SS} | | 0.25 | V |
| | Analog input pin | | | | - | |
| V _{Analog} | Input voltage range | 4) | Vss | | Vcc | V |
| F _{Sample} | Sample rate | 5) | 0.002 | | 500 | Sample/s |
| | Counter input pin | | | | | |
| F _{Counter} | Input frequency | | | | 1000 | Hz |
| | Synchronous serial timing | | | | | |
| SCLK freq. | Synchronous clock frequency (byte mode) | | 285 | 300 | 315 | kHz |
| $t_{ReadValid}$ | Data is valid on read before low-to-high transition on the clock (byte mode) | | 0.5 | | | μs |
| t _{WriteValid} | Data must be valid on write within this time after a high-to-low transition on the clock (byte mode) | | | | 2 | μs |
| t_{SRDY} _MinLow | Minimum SRDY low time | | 2.5 | | | μs |
| t _{Reset} | Synchronous reset. SRDY falling edge to MRDY falling edge | | 250 | | | μs |
| | General RF conditions | _ | | _ | | |
| f _{OP} | Operating frequency | 1) | 2400 | | 2524 | MHz |
| F _{Channel} | Channel spacing | -/ | 2.00 | 1 | | MHz |
| Δf | Frequency deviation | | | ±156 | | kHz |
| | Current consumption | | | | | |
| I _{Idle} | No active channels – no communications | | | 1.1 | | μA |
| I _{Suspend} | Asynchronous suspend activated | | | 1.1 | | μA |
| I _{Base} | Base active current | | | 2.6 | | μA |
| I _{sample} | Average current/analog sample | | | 0.5 | | μA |
| I _{SC RF} | Average current/ ANT message in sensRcore mode | | | 13 | | μA |
| | | | | | | |
| I _{Msg_Rx_ByteSync} | Average current / Rx message in byte sync mode | | | 10.5 | | μA |
| I _{Msg_Rx_BitSync} | Average current / Rx message in bit sync mode | | | 13.1 | | μA |

Z

Conditions: V_{CC} = +2.0V, V_{SS} = 0V, T_A = - 40°C to +85°C



| Symbol | Parameter (condition) | Notes | Min | Тур | Max | Units |
|--------------------------------------|--|-------|-----|------|---------|----------|
| I _{Msg_Rx_57600} | Average current / Rx message in async mode at 57600 baud | | | 9.1 | | μA |
| I _{Msg_Rx_19200} | Average current / Rx message in async mode at 19200 baud | | | 10.4 | | μA |
| I _{Msg_Rx_4800} | Average RF current / Rx message in async mode at 4800 baud | I | | 8.5 | | μA |
| I _{Msq Tx ByteSync} | Average current / Tx-only message in byte sync mode | | | 6.4 | | μA |
| I _{Msq Tx BitSync} | Average current / Tx-only message in bit sync mode | | | 10.8 | | μA |
| I _{Msg_Tx_57600} | Average current / Tx-only message in async mode at 57600 baud | | | 5.7 | | μA |
| I _{Msg_Tx_19200} | Average current / Tx-only message in async mode at 19200 baud | | | 7.5 | | μA |
| I _{Msg_Tx_4800} | Average current / Tx-only message in async mode at 4800 baud | | | 4.4 | | μA |
| | | | | | | |
| I _{Msq TR ByteSync} | Average current / Tx message in byte sync mode | | | 14.1 | | μA |
| I _{Msq TR BitSync} | Average current / Tx message in bit sync mode | | | 18.4 | | μA |
| I _{Msg_TR_57600} | Average current / Tx message in async mode at 57600 baud | | | 13.5 | | μA |
| I _{Msg_TR_19200} | Average current / Tx message in async mode at 19200 baud | | | 15.0 | | μA |
| I _{Msg_TR_4800} | Average current / Tx message in async mode at 4800 baud | | | 11.7 | | μA |
| | | | | | | |
| I _{Msg_Ack_ByteSync} | Average current / Acknowledged message in byte sync mode | L | | 19.6 | | μA |
| I_{Msg} Ack_BitSync | Average current / Acknowledged message in bit sync mode | | | 23.4 | | μA |
| I _{Msg_Ack_57600} | Average current / Acknowledged message in async mode at 57600 baud | | | 18.7 | | μA |
| I _{Msg_Ack_19200} | Average current / Acknowledged message in async mode at 19200 baud | | | 19.9 | | μA |
| I _{Msg_Ack_4800} | Average current / Acknowledged message in async mode at 4800 baud | L | | 17.2 | I | μA |
| T | Deal Current consumption | | _ | 10 | | |
| I _{Peak} | Peak Current consumption | | | 19 | | mA |
| I _{PeakTx} | Peak Current – Tx-only @ 0dBm | | | 13 | | mA |
| I _{Ave} | Broadcast Tx-only @ 0.5Hz in byte sync mode | | | 5.8 | | μA |
| | Broadcast Tx-only @ 2Hz in byte sync mode | | | 15.4 | | μΑ |
| I _{Ave} | Broadcast Rx @ 0.5Hz in byte sync mode | | | 7.8 | | μΑ |
| I _{Ave} I _{Ave} | Acknowledged @ 0.5Hz in byte sync mode | | | 12.4 | | μΑ |
| | Burst continuous @ 14Kbps in byte sync mode | | | 2.24 | | μA mA |
| I _{Ave} T. | Burst continuous @ 20Kbps in byte sync mode | | | 3.24 | | mA |
| I _{Ave} | Burst continuous @ 20Kbps in byte sync mode | | | 3.21 | | mA |
| I _{Ave} I _{Ave} | Burst continuous @ 14Kbps in async mode at 57600 | | | 2.37 | | mA |
| I _{Ave} | baud Burst continuous @ 20Kbps in async mode at 57600 | | | 3.31 | | mA |
| | baud Transmitter operation | | | | | |
| P _{RF} | Maximum output power | 2) | | 0 | 4 | dBm |
| ΔΡ | Output power variation | 3) | | 5 | + ±4 | dBm |
| P _{BW} | 20dB bandwidth for modulated carrier | 5) | | | 1000 | kHz |
| P _{BW} P _{RF2} | 2 nd adjacent channel transmit power 2MHz | | | | -20 | dBm |
| | 3 rd adjacent channel transmit power 3MHz | | | | -20 | |
| P _{RF3} | | | | 11.3 | -40 | dBm |
| Ivcc | Supply peak current @ 0dBm output power | | | | | mA |
| Ivcc | Supply peak current @ -20dBm output power Receiver operation | | | 7 | | mA |

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| Symbol | Parameter (condition) | Notes | Min | Тур | Max | Units |
|--------------------|---|-------|-----|-----|-----|-------|
| I _{VCC} | Supply peak current receive mode | | | 12 | | mA |
| RX _{SENS} | Sensitivity at 0.1%BER (@1000kbps) | | | -85 | | dBm |
| C/I _{CO} | C/I co-channel | | | 9 | | dB |
| C/I _{1ST} | 1 st adjacent channel selectivity C/I 1MHz | | | 8 | | dB |
| C/I _{2ND} | 2 nd adjacent channel selectivity C/I 2MHz | | | -22 | | dB |
| C/I _{3RD} | 3 rd adjacent channel selectivity C/I 3MHz | | | -30 | | dB |

1) Usable band is determined by local regulations.

2) Maximum output power with 0dBm output power setting.

3) Variation from 2402MHz to 2479MHz.

4) Voltages exceeding the reference can be used but provide no information.

5) Max refers to total number of samples available to be distributed over the number of A/D sources currently active.

3.1 Current Calculation Examples

1. Master channel with Broadcast data at 4Hz with a bit synchronous serial interface.

 $I_{ave} = (I_{Msg_Tx_BitSync} * Message_Rate) + I_{Base}$ $= (18.4 \ \mu A/message * 4 \ messages) + 2.6 \ \mu A$ $= 76.2 \ \mu A$

2.Receive channel with Acknowledged data at 2Hz with an asynchronous serial interface at 57 600 baud.

$$I_{ave} = (I_{Msg_Ack_57600} * Message_Rate) + I_{Base}$$
$$= (18.7\mu A/message * 2 messages) + 2.6\mu A$$
$$= 40.0\mu A$$

3. Transmit channel with Acknowledged data at 2Hz with an asynchronous serial interface at 57 600 baud.

$$I_{ave} = (I_{Msg_Ack_57600} * Message_Rate) + I_{Base}$$
$$= (18.7 \ \mu A/message * 2 messages) + 2.6 \mu A$$
$$= 40.0 \mu A$$

4.SensRcore device using an ANT message rate of 4Hz and sampling an A/D input at 16 Hz.

$$I_{ave} = (I_{SC_{RF}} * Message_Rate) + (I_{Sample} * Sample_Rate) + I_{Base}$$
$$= (13\mu A/message * 4 messages) + (0.5\mu A/sample * 16 samples) + 2.6\mu A$$
$$= 62.6\mu A$$

3.2 A/D Specifications

These are taken from the TI MSP430x22x4 datasheet:



10-bit ADC, power supply and input range conditions (see Note 1)

| | PARAMETER | TEST CONDITIONS | ТА | VCC | MIN | TYP | MAX | UNIT |
|-----------------|--|---|--------------|-------|-----|------|-----------------|------|
| Vcc | Analog supply voltage range | V _{SS} = 0 V | | | 2.2 | | 3.6 | v |
| V _{Ax} | Analog input voltage range (see Note 2) | All Ax terminals. Analog inputs selected in ADC10AE register. | | | 0 | | V _{CC} | v |
| IADC10 | ADC10 supply current | fADC10CLK = 5.0 MHz ADC10ON = 1, REFON = 0 ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0 | l: -40-85°C | 2.2 V | | 0.52 | 1.05 | |
| | (see Note 3) | | T: -40-105°C | 3 V | | 0.6 | 1.2 | mA |

NOTES: 1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.

The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
 The internal reference supply current is not included in current consumption parameter I_{ADC10}.

The internal reference current is supplied via terminal V_{CC}. Consumption parameter (ADC10)
 The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC100N control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-bit ADC, built-in voltage reference

| | PARAMETER | TEST CONDITIONS | VCC | MIN | TYP | MAX | UNIT |
|----------|---|--|-----------|------|-----|------|------|
| | Positive built-in reference analog F+ supply voltage range | IVREF+≤ 1mA, REF2_5V=0 | | 2.2 | | | |
| VCC.REF+ | | IVREF+ ≤ 0.5mA, REF2_5V=1 | | 2.8 | | | v |
| | | IVREF+≤ 1mA, REF2_5V=1 | | 2.9 | | | |
| | Desitive built in reference veltage | IVREF+≤IVREF+max, REF2_5V=0 | 2.2 V/3 V | 1.41 | 1.5 | 1.59 | V |
| VREF+ | | I _{VREF+} ≤ I _{VREF+} max, REF2_5V=1 | 3 V | 2.35 | 2.5 | 2.65 | V |

10-bit ADC, linearity parameters

| | PARAMETER | TEST CONDITIONS | VCC | MIN | түр | MAX | UNIT |
|----|------------------------------|--|---|-----|---|--|------|
| El | Integral linearity error | | 2.2 V/3 V | | | ±1 | LSB |
| ED | Differential linearity error | | 2.2 V/3 V | | | ±1 | LSB |
| EO | Offset error | Source impedance $R_S \le 100 \Omega$, | 2.2 V/3 V | | | ±1 | LSB |
| EG | | SREFx = 010; un-buffered external reference; VeREF+ = 1.5V | 2.2 V | | ±1.1 | ±2 | LSB |
| | | SREFx = 010; un-buffered external reference; VeREF+ = 2.5V | 3 V | | ±1.1 | ±2 | LSB |
| EG | Gain error | SREFx = 011; buffered external reference (see Note 1); V _{eREF+} = 1.5V | 2.2 V | | ±1.1 | ±1 ±1 1 ±2 1 ±2 1 ±2 1 ±2 1 ±4 2 ±5 2 ±5 2 ±5 2 ±7 | LSB |
| | | SREFx = 011; buffered external reference (see Note 1); VeREF+ = 2.5V | 3 V | | ±1 ±1 ±1.1 ±2 ±1.1 ±2 ±1.1 ±2 ±1.1 ±2 ±1.1 ±3 ±1.1 ±3 ±2 ±5 ±2 ±5 ±2 ±5 | LSB | |
| | | SREFx = 010; un-buffered external reference; V _{eREF+} = 1.5V | 2.2 V | | ±2 | тą | LSB |
| | | SREFx = 010; un-buffered external reference; V _{eREF+} = 2.5V | $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | LSB | | | |
| ET | Total unadjusted error | SREFx = 011; buffered external reference (see Note 1); V _{eREF+} = 1.5V | 2.2 V | | ±2 | ±7 | LSB |
| | | SREFx = 011; buffered external reference (see Note 1); V _{eREF+} = 2.5V | 3 V | | ±2 | ±6 | LSB |

NOTES: 1. The reference buffer's offset adds to the gain and total unadjusted error.

3.3 Reflow Guideline

Follow the guideline below if ANT11TxxM4IB modules go through reflow oven.

Peak solder joint/pad temperatures exceeding 240°C are not recommended.

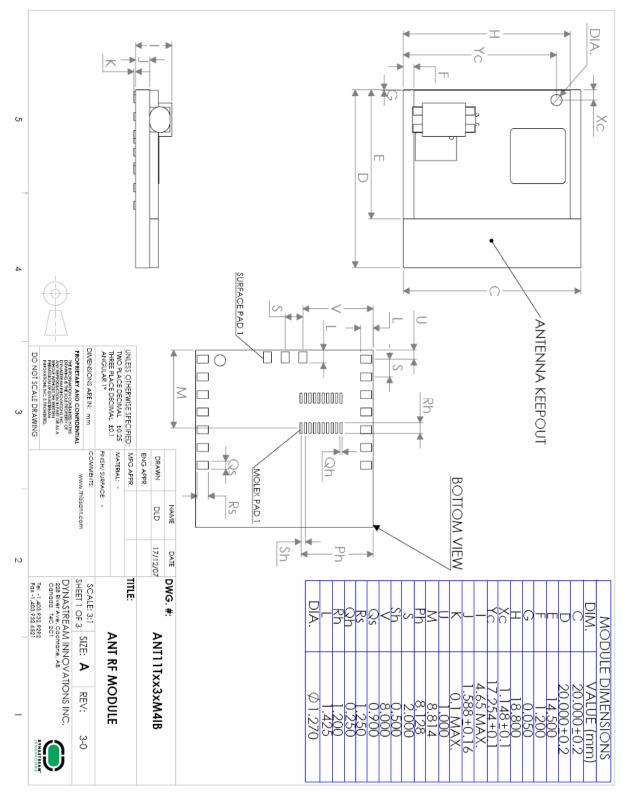
If possible, pre-heat the assembly within the oven profile for \sim 30 seconds at \sim 150 °C.

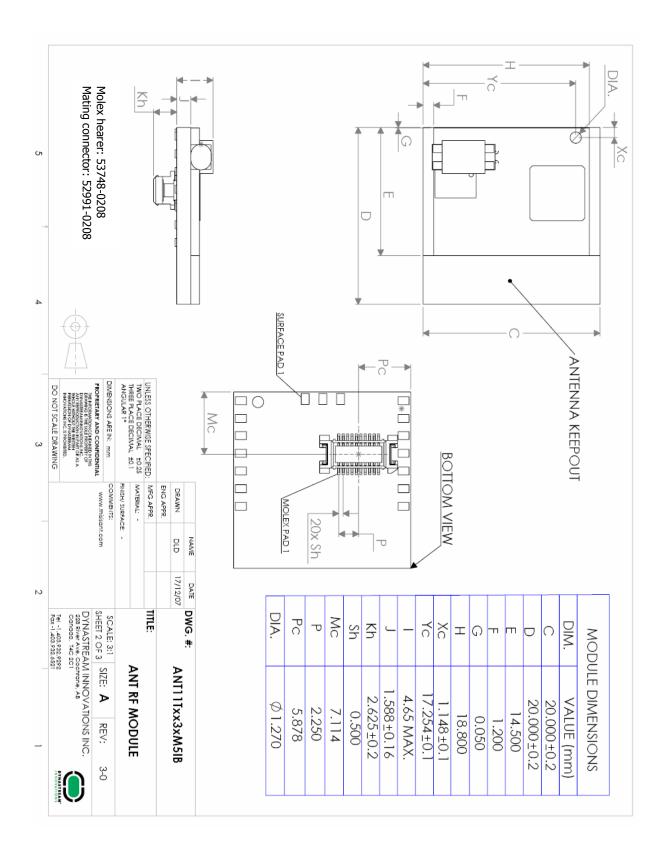


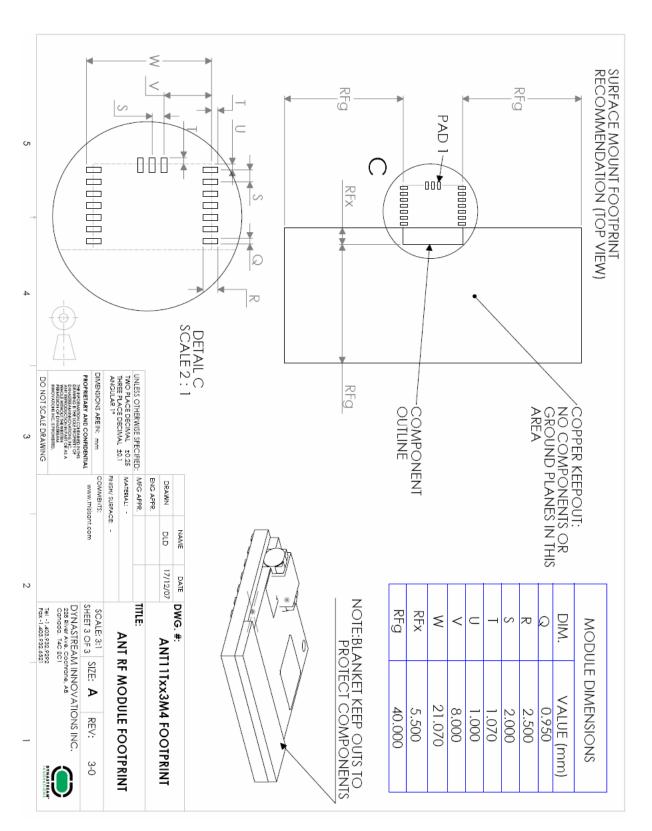
Follow the solder paste manufacturer's recommendations, especially regarding temperature ramp rate and the time above liquidus.

Ζ

4 Mechanical Drawings







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4.1 Connection Diagram

